IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Appl. No.	:	10/681,068	Confirmation No. : 8619
Appellant	:	Andrew S. Hildebrant, et al.	
Filed	:	October 7, 2003	
TC/A.U.	:	3714	
Examiner	:	Frank M. Leiva	
Docket No.	:	10030549-1	

Mail Stop Appeal Brief – Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

APPEAL BRIEF

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APPEAL BRIEF

Dear Sir:

This Appeal Brief is submitted in response to the Examiner's Final Office Action mailed March 15, 2010. The fee for filing this Appeal Brief was paid with a previous appeal attempt. Of note, this is the fourth Appeal Brief that appellants have filed – each of which has addressed new art rejections. Each of the past three Appeal Briefs has been followed by the Examiner's re-opening of prosecution.

Appellants filed a Notice of Appeal and Pre-Appeal Brief by mail on June 15, 2010, which Notice of Appeal was received by the Office on June 21, 2010. A Notice of Panel Decision from Pre-Appeal Brief Review was mailed July 12, 2010.

This Appeal Brief is believed to be timely submitted within the two-month response deadline, because it is being transmitted to the USPTO via EFS on October 21, 2010 in the jurisdiction from which it is being transmitted, along with a Certificate of Transmission, as provided for in 37 CFR 1.8 and the notice published in the Federal Register, Vol. 72, No. 14.

Certificate of Transmission Under 37 CFR 1.8

I hereby certify that this correspondence is being transmitted to the United States Patent and Trademark Office, via EFS, on October 21, 2010.

_____/Gregory W. Osterloth/_____
Gregory W. Osterloth

Real Party in Interest

The real party in interest is Verigy (Singapore) Pte. Ltd., a Singaporean limited liability company.

Related Appeals and Interferences

The rejections of the claims in United States patent application no. 10/666,024 have been appealed to the Board of Patent Appeals and Interferences. The decision on this appeal was previously thought to have some relevance to the appeal of the rejections in the instant application, because the claims of the instant application were previously rejected on the same basis as the claims in application no. 10/666,024. However, those rejections were overcome in the instant application, and appellants believe the decision on appeal for application no. 10/666,024 is probably now less relevant to the instant appeal.

Status of Claims

Claims 1-17 are pending, all of which stand rejected. The rejections of claims 1-17 are appealed.

A copy of the claims is attached as a Claims Appendix to this Appeal Brief.

Status of Amendments

No amendments were made to the claims subsequent to final rejection. All amendments have been entered.

Summary of Claimed Subject Matter

In a first embodiment (claim 1) a machine-executable method comprises executing sequences of instructions on a machine (p. 9, lines 1-11), the executed sequences of instructions causing the machine to perform the actions of 1) reading a test file having a plurality of test vectors (p. 5, lines 10-18; FIG. 2, 200), 2) determining a required memory needed to execute the plurality of test vectors (p. 5, line 19 - p. 6, line 13; FIG. 2, 205), and 3) using the required memory to estimate a cost to execute the test vectors (p. 6, lines 14-20; FIG. 2, 210).

In a second embodiment (claim 8), a system (p. 4, lines 3-4; FIG. 1, 100) comprises a machine programmed to execute sequences of instructions (p. 9, lines 1-11), wherein execution of the sequences of instructions defines 1) logic (FIG. 1, 102) to read a test file having a plurality of test vectors (p. 4, lines 5-6; p. 5, lines 10-18) and to determine a required memory needed to execute the plurality of test vectors (p. 4, lines 5-7; p. 5, line 19 - p. 6, line 13), and 2) a billing predictor (p. 4, lines 8-14; p. 6, lines 14-20; FIG. 1, 104), communicatively coupled to the logic, to use the required memory to estimate a cost to execute the test vectors.

In a third embodiment (claim 13), one or more machine-readable mediums have sequences of instructions stored thereon (p. 9, lines 5-10). When executed by a machine, the sequences of instructions cause the machine to perform the following actions: 1) read a test file having a plurality of test vectors (p. 5, lines 10-18; FIG. 2, 200); 2) determine a required memory needed to execute the plurality of test vectors (p. 5, line 19 - p. 6, line 13; FIG. 2, 205); and 3) use the required memory to estimate a cost to execute the test vectors (p. 6, lines 14-20; FIG. 2, 210).

Grounds of Rejection to be Reviewed on Appeal

1. Whether claims 1-5 and 7-16 should be rejected under 35 USC 102(b) as being anticipated by Agrawal (US 5,257,268).

2. Whether claims 6 and 17 should be rejected under 35 USC 103(a) as being unpatentable over Agrawal.

Argument

1. Claims 1-5 and 7-16 should not be rejected under 35 USC 102(b) as being anticipated by Agrawal (US 5,257,268).

Claim 1 recites:

> 1. A machine-executable method comprising:
> executing sequences of instructions on a machine, the executed sequences of instructions causing the machine to perform the actions of,
> reading a test file having a plurality of test vectors;
> determining a required memory needed to execute the plurality of test vectors; and
> using the required memory to estimate a cost to execute the test vectors.

With respect to claim 1, the Examiner asserts that Agrawal discloses "determining a required memory needed to execute [a] plurality of test vectors" in col. 4:40-60, where Agrawal discloses a system that determines "the minimum required number of flip-flops gates (memory)". *See*, 3/15/2010 Final Office Action, p. 4. Appellants respectfully disagree.

Agrawal discloses that:

> . . .A sequential circuit. . .is fully initialized when all its memory elements are in known states. One has to provide a set of initialization vectors to bring a circuit to a known state, and those initialization vectors must be chosen appropriately. In accordance with our preferred embodiment, the initialization vectors are generated by a procedure that minimizes a "cost function". We chose our cost function to correspond to the number of flip-flops in the "unknown" state, but other cost functions are also possible.
>
> As shown in the flow chart of FIG. 2, the initialization process begins at block 100 with the assumption that all flip-flops are at the "unknown" state, and the cost function is simply equal to the number of flip-flops in the circuit, M. The process of selecting a set of initialization vectors consists of generating "trial vectors" and accepting only those trial vectors that reduce the cost.

Col. 4, lines 43-60.

From the above excerpt, appellants believe it is clear that Agrawal does not

disclose an action of "determining a required memory needed to execute [a] plurality of test vectors", as the Examiner asserts. Instead, Agrawal discloses how to determine what vectors are needed to initialize the flip-flops of a circuit under test. Agrawal does this by first setting up a cost function and initializing it to some value, such as the number of flip-flops in the circuit that are in an unknown state. AFTER setting up the cost function, Agrawal generates or selects a "trial vector", and simulates its application to the circuit to be tested. After application of the trial vector to the circuit, Agrawal counts the number of flip-flops that remain in an unknown state and compares this count to the value of the cost function. If the value of the cost function (i.e., the "total cost") is reduced, the trial vector is saved as an initialization vector, and a different trial vector is selected or generated and applied to the circuit. Only those trial vectors that reduce the value of the cost function are added to the set of initialization vectors. When the cost function reaches zero, or falls below some preset threshold, the set of initialization vectors is deemed complete. *See*, e.g., Agrawal's FIG. 2 and col. 4:61 - 5:68.

Of note, Agrawal never determines the "required memory needed to execute" the set of initialization vectors. Rather, Agrawal applies each of a number of trial vectors to a circuit (without determining a required memory needed to execute any of the trial vectors), and after each application makes a determination of how many flip-flops remain in an unknown state (again, without determining a required memory needed to execute any of the trial vectors). Agrawal's application of trial vectors, and iterative assessment of the number of flip-flops remaining in an unknown state, continues until the number of flip-flops remaining in an unknown state falls below a certain value (or is equal to zero). However, Agrawal never determines a required memory needed to execute the trial vectors (or even one of the trial vectors). Instead, Agrawal determines a required number of trial vectors to initialize a fixed number of flip-flops in a circuit.

In the Comments attached to the Notice of Panel Decision form Pre-Appeal Brief Review mailed July 12, 2010, the Examiner asserts for the first time that:

Determination of required memory (claim 1) is located in Agrawal column 5

> lines 12-36, where after simulating executing the test vector the system counts the flip-flops (or memory units) that remained unknown, or in simple terms calculating the memory not used. ***Total memory minus unknown memory equals required memory to execute the test vector.***

Although the emphasized statement in the above excerpt is true, it is not disclosed by Agrawal. Rather, it is a deduction made by the Examiner in light of what is disclosed in appellants' specification. Furthermore, it is noted that appellants' claim 1 recites "determining a required memory needed to execute ***the plurality*** of test vectors", which would require even more processing that is not disclosed by Agrawal.

Given that Agrawal does not disclose "determining a required memory needed to execute the plurality of test vectors", it follows that Agrawal cannot disclose "using the required memory to estimate a cost to execute the test vectors." In particular, the "cost function" disclosed by Agrawal is not "a cost to execute. . .[a plurality of] test vectors". Instead, Agrawal's "cost function" is an optimization function that is used to limit growth in a set of initialization vectors. For example, in a simple case, an initialization vector is not added unless it actually causes additional flip-flops to be initialized optimum number of initialization vectors.

In the Comments attached to the Notice of Panel Decision form Pre-Appeal Brief Review mailed July 12, 2010, the Examiner notes that:

> It is the examiner's position that the Agrawal reference not only simulates execution of a tests vector and calculates the cost of executing it, but reduces the overall cost of testing the circuit by continually running trial tests vectors to find the most efficient vector.

Appellants have already explained, *supra*, that Agrawal does not calculate the cost of executing a test vector. In addition, appellants disagree with the latter part of the Examiner's above assertion. That is, there is no disclosure by Agrawal that the overall cost of testing a circuit is reduced by continually running trial test vectors to find the most efficient vector. Rather, Agrawal determines whether each of a number of test vectors reduces the cost function associated with a current set of initialization vectors. The cost function is not equivalent to the cost of executing the initialization

vectors, but is instead equal to the number of flip-flops that cannot be exercised by the current set of initialization vectors.

Because Agrawal does not disclose each and every recitation of appellants' claim 1, appellants believe the Examiner has committed clear error, and claim 1 is believed to be allowable.

Claims 2-5 and 7 are believed to be allowable, at least, because they depend from claim 1.

Claims 8-16 are believed to be allowable, at least, for reasons similar to why claim 1 is believed to be allowable.

Claims 3, 10 and 15 are also believed to be allowable because Agrawal fails to disclose that "determining a required memory comprises determining a required memory needed for ***each of a plurality of boards of a tester*** to execute the test vectors for the board." The Examiner asserts that this is disclosed in Agrawal's col. 6:50-68, in that Agrawal's "levels" of flip-flops are equivalent to different "boards of a tester". Appellants wholeheartedly disagree. Agrawal's levels correspond to: flip-flops at primary outputs of a circuit; flip-flops feeding into the primary outputs; flip-flops feeding combinational logic that does not drive the primary outputs; etc. Nothing in Agrawal's levels of flip-flops connotes or suggests "a plurality of boards of a tester".

Claims 4, 11 and 16 are also believed to be allowable because Agrawal fails to disclose that "determining a required memory comprises determining a required memory needed for each of a plurality of pins of a tester to execute the test vectors for the pin." The Examiner asserts that this is disclosed in Agrawal's col. 1:16-30, where Agrawal discloses that a circuit can have multiple inputs and outputs. However, nowhere does Agrawal disclose that a required memory is determined for "each" of these inputs or outputs, or that a required memory is determined for each pin "of a tester". Instead, Agrawal's disclosure at col. 4:61 - 5:68 indicates that a set of initialization vectors is determined for a circuit as a whole.

Claims 5 and 12 are also believed to be allowable because Agrawal fails to disclose that "determining a required memory comprises counting the number of test vectors for each of one or more tests in the test file." The Examiner asserts that this

is taught by Agrawal in col. 4:49-68. Appellants disagree. Agrawal only discloses test vectors, and does not indicate that a number of test vectors correspond to "each of one or more tests in [a] test file."

2. Claims 6 and 17 should not be rejected under 35 USC 103(a) as being unpatentable over Agrawal.

Appellants' claims 6 and 17 are believed to be allowable, at least, because they respectively depend from claims 1 and 13. In addition, appellants assert that Agrawal is devoid of any disclosure pertaining to what is recited in claims 6 and 17. In particular, Agrawal fails to disclose "determining a first memory requirement needed for ***a first pin of a tester*** to execute the test vectors for a first test in the test file"; "determining a second memory requirement needed for [an] ***additional pin*** to execute the test vectors for the first test"; and "if the second memory requirement is greater than the first memory requirement, setting the required memory equal to the second memory requirement." Agrawal's comparisons of cost function values has nothing to do with comparing memory requirements.

3. Conclusion

In summary, the art of record does not teach nor suggest the subject matter of appellant's claims 1-17. These claims are therefore believed to be allowable.

Respectfully submitted,
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Claims Appendix

1. A machine-executable method comprising:

executing sequences of instructions on a machine, the executed sequences of instructions causing the machine to perform the actions of,

reading a test file having a plurality of test vectors;

determining a required memory needed to execute the plurality of test vectors; and

using the required memory to estimate a cost to execute the test vectors.

2. The method of claim 1, wherein the executed sequences of instructions further cause the machine to perform the action of receiving a billing scheme; wherein using the required memory to estimate a cost includes using the billing scheme to estimate the cost to execute the test vectors.

3. The method of claim 1, wherein determining a required memory comprises determining a required memory needed for each of a plurality of boards of a tester to execute the test vectors for the board.

4. The method of claim 1, wherein determining a required memory comprises determining a required memory needed for each of a plurality of pins of a tester to execute the test vectors for the pin.

5. The method of claim 1, wherein determining a required memory comprises counting the number of test vectors for each of one or more tests in the test file.

6. The method of claim 1, wherein determining a required memory comprises:

determining a first memory requirement needed for a first pin of a tester to execute the test vectors for a first test in the test file;

setting the required memory equal to the first memory requirement; and

for each additional pin of the tester,

determining a second memory requirement needed for the additional pin to execute the test vectors for the first test; and

if the second memory requirement is greater than the first memory requirement, setting the required memory equal to the second memory requirement.

7. The method of claim 6, wherein the executed sequences of instructions further cause the machine to perform the action of, for each additional test in the test file:

for each pin of the tester, determining a third memory requirement for the pin to execute the test vectors for the additional test; and setting the required memory equal to the third memory requirement if the third memory requirement is greater than the required memory.

8. A system comprising:

a machine programmed to execute sequences of instructions, wherein

execution of the sequences of instructions defines,

logic to read a test file having a plurality of test vectors and to determine a required memory needed to execute the plurality of test vectors; and

a billing predictor, communicatively coupled to the logic, to use the required memory to estimate a cost to execute the test vectors.

9. The system of claim 8, wherein the machine further comprises a user interface to display the cost to a user.

10. The system of claim 8, further comprising a tester having a plurality of boards; wherein the logic is to determine a required memory needed for each board of the tester to execute the test vectors for the board.

11. The system of claim 8, further comprising a tester having a plurality of boards, each board including a plurality of pins; wherein the logic is to determine a required memory needed for each pin to execute the test vectors for the pin.

12. The system of claim 8, wherein the logic is to determine the required memory by counting the number of test vectors for each test in the test file.

13. One or more machine-readable mediums having stored thereon sequences of instructions, which, when executed by a machine, cause the machine to perform the actions:

reading a test file having a plurality of test vectors;

determining a required memory needed to execute the plurality of test vectors; and

using the required memory to estimate a cost to execute the test vectors.

14. The machine-readable mediums of claim 13, further comprising instructions, which when executed by the machine, cause the machine to perform the actions of receiving a billing scheme; and wherein the instructions for using the required memory to estimate a cost include instructions, which when executed by the machine, cause the machine to perform the actions of using the billing scheme to estimate the cost to execute the test vectors.

15. The machine-readable mediums of claim 13, wherein the instructions for determining a required memory comprise instructions, which when executed by the machine, cause the machine to perform the actions of determining a required memory needed for each of a plurality of boards of a tester to execute the test vectors for the board.

16. The machine-readable mediums of claim 13, wherein the instructions for determining a required memory comprise instructions, which when executed by the machine, cause the machine to perform the actions of determining a required memory needed for each of a plurality of pins of a tester to execute the test vectors for the pin.

17. The machine-readable mediums of claim 13, wherein the instructions for determining a required memory comprise instructions, which when executed by the machine, cause the machine to perform the actions:

determining a first memory requirement needed for a first pin of a tester to execute the test vectors for a first test in the test file;

setting the required memory equal to the first memory requirement; and

for each additional pin of the tester,

determining a second memory requirement needed for the additional pin to execute the test vectors for the first test; and

if the second memory requirement is greater than the first memory requirement, setting the required memory equal to the second memory requirement.

Evidence Appendix

None.

Related Proceedings Appendix

None.